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Michael B. Atlass
Unisys Corporation
Unisys Way, MS/E8-114
Blue Bell, PA 19424-0001

EXAMINER	
ZHE, MENG YAO	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/715,699	GEYE ET AL.	
	Examiner	Art Unit	
	MengYao Zhe	2109	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11/18/2003* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-36 are presented for examination.

Specification

2. The abstract of the disclosure is objected to because the abstract does not support the claims. In other words, what is being claimed is written in such a way that is not properly reflected in the abstract. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-36 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

A. The following claim languages are not clear and indefinite:

i) Claim 25, lines 1-2, it is unclear what the relationship is between "a system" in line 1 and "the multiprocessor system" in line 2 <i.e. are they the same system?>.

Line 3, it is uncertain whether "a processor" in line 3 refers to "a processor" in line 1 <i.e. if they are the same, "the" or "said" should be used.>. Furthermore, while line 2 claims for "a multiprocessor system", only one processor is claimed in line 3.

Line 4, it is not clearly indicated as to what the word "bearing" means <i.e. are the computer-readable instructions stored in the memory?>. It is also unclear what the relationship are among "a computer-readable memory", "a system" in line 1, and "a multiprocessor system" in line 2 <i.e. does the memory belong to the system or the multiprocessor system?>.

Line 6, it is unclear what the relationship is between "a first set of computer-readable instructions" and "a set of computer-readable instructions" in line 1 <I.e. are there multiple sets? Or is the set mentioned in line 6 the same set as that in line 1?>.

Line 7, it is not clearly understood what the relationship is between "a first cluster", "a system" in line 1, and "a multiprocessor system" in line 2 <i.e. is the cluster part of the system or the multiprocessor system?>.

Line 8, it is not clearly understood what the "priority indicator" is indicating <i.e. is it indicating priorities of the instructions or the priority of the processors?>.

Also it is unclear who assigns the priority. It is unclear what "a function" is < i.e. higher the priority associated with a cluster means higher probability that a cluster gets selected?>.

Lines 10-12: it is unclear what the relationship is between "a first processor" and "a processor" in line 3. It is unclear what the relationships are among "the cluster" in line 10, "a first cluster" in line 7, and "the selected cluster" in lines 8 <i.e. are they all the same cluster?>. It is unclear what the "priority indicator" is indicating. It is unclear what the relationship is between "an associated priority indicator" in line 11 and "an associated priority indicator" in line 8. Also it is unclear who or what is assigning the priority. It is unclear what "a function" is.

Lines 6, 7, 10, and 13: It is not clearly indicated as to who performs the "selecting" and the "associating" steps <i.e. how could a memory alone perform a step? Is it the computer-readable instructions in line 5 that performs this?>.

Claims 1 and 13 have the same deficiencies as claim 25 above.

ii) Claim 26, line 1, it claims for processors--more than one processor--while only one processor is claimed in line 2 of claim 25.

Claims 2 and 14 have the same deficiencies as claim 26 above.

iii) Claim 29, lines 2-3, It is unclear what the relationship is between "the priority of each selected set of computer-readable instructions" and "an

associated priority indicator" in line 11 of claim 25 <i.e. line 11 of claim 25 is a priority indicator for processors, not instructions> It is also unclear what "a function" is and how it is related to the functions found in claim 25 < i.e. are they all the same function?>.

Claims 5 and 17 have the same deficiencies as claim 29 above.

iv) Claims 30, 31, It is unclear what the relationship is between "the priority of each selected set of computer-readable instructions" and "a associated priority indicator" in line 11 of claim 25. It is also unclear what "a function" is and how it is related to the functions found in claim 25.

Claims 6, 7, 18, 19 have the same deficiencies as claims 30 and 31 above, respectively.

v) Claim 32, it is not clearly indicated how "the step of adjusting the priority based on the priority of the first set of computer-readable instructions" is performed <i.e. is it increasing or decreasing the priority using the priority of the first set of computer-readable instructions?>.

Claims 8 and 20 have the same deficiencies as claim 32 above.

vi) Claim 35, line 2-3, it is unclear what the relationship is between "the other cluster" in line 2 and "the other cluster" in line 3 <i.e. are they the same other cluster?>. It is unclear how the other cluster can have a processor and not have a processor associated with the first set of computer-readable instructions. It is

also unclear what the relationship is between "the other cluster" and "a cluster other than the first cluster" in line 1 < i.e. are they the same cluster?>

Claims 11 and 23 have the same deficiencies as claim 35 above.

vii) Claim 36, it is unclear what the relationship is between "the other processor" in line 3 and "a processor other than the first processor" in lines 1-2 <i.e. are they the same processor?>.

Claims 12 and 24 have the same deficiencies as claim 26 above.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-36 are rejected under 35 U.S.C 102(b) as being anticipated by Kimmel et al., Patent No. 6,105,053 (hereafter Kimmel).

7. As per claim 1, Kimmel teaches the invention as claimed including a method of associating a processor with a set of computer-readable instructions in a multiprocessor system, comprising:

selecting a first set of computer-readable instructions (Col 6, lines 54-61);

selecting a first cluster from at least two clusters (Fig 1A: all JP that routes to the same shared memory corresponds to a cluster. For example, JP0 and JP1 make up one cluster.), each cluster having an associated priority indicator, where the selected cluster is selected as a function of its priority indicator (Col 9, lines 28-38: each node on level 1, which corresponds to a cluster, gets its own run queue. Col 6, lines 10-15, 54-61: each thread group has its own priorities. Each queue in all of the node levels contains the thread groups and their associated priorities. Thus each node on level 1 will have priority values associated with it. Col 13, line 40-Col 14, line 27; Col 15, line 1, Col 16, lines 35-47: load value for each node can be measure using priorities found in its queues, which can then be used by the scheduler perform load balancing among any nodes at any level, thus selecting a node to execute a thread group when other nodes are overloaded);

selecting a first processor from the cluster, the cluster comprising at least two processors (Fig 1B, node 110 corresponds to a cluster, unit 100 and 101 are processors.), each processor having an associated priority indicator, where the selected processor is selected as a function of its priority indicator (Col 13, line 40-Col 14, line 27; Col 15, line 1, Col 16, lines 35-47);

associating the first processor with the first set of computer-readable instructions (Col 13, line 40-Col 14, line 27).

8. As per claim 2, Kimmel teaches wherein the processors comprise CPUs (Fig 1A; Col 5, lines 15-21).

9. As per claim 3, Kimmel teaches wherein the first set of computer-readable instructions comprise an application program (Col 5, line 60 to Col 6, line 5: computer-readable instructions are application programs).

10. As per claim 4, Kimmel teaches wherein the first set of computer-readable instructions comprise an processing thread (Col 5, line 60 to Col 6, line 5).

11. As per claim 5, Kimmel teaches wherein the priority indicator associated with each processor is a function of the priority of each selected set of computer-readable instructions associated with the processor (Col 9, lines 28-38; Col 6, lines 10-15, 54-61; Col 13, line 40-Col 14, line 27; Col 15, line 1, Col 16, lines 35-47).

12. As per claim 6, Kimmel teaches wherein the priority indicator for each cluster is a function of the priority of each processor in the cluster (Col 9, lines 28-38; Col 6, lines 10-15, 54-61; Col 13, line 40-Col 14, line 27; Col 15, line 1, Col 16, lines 35-47: the load of the level 1 nodes are based on the sub-tree beneath it. Since the processors are level 0, below level 1 of the clusters, priority of level 1 is a function of priority of level 0).

13. As per claim 7, Kimmel teaches wherein the priority indicator for each cluster is a function of the priority of each processor in the cluster (Col 9, lines 28-38; Col 6, lines 10-15, 54-61; Col 13, line 40-Col 14, line 27).

14. As per claim 8, Kimmel teaches the step of adjusting the priority of the selected processor based on the priority of the first set of computer-readable instructions (Col 9, lines 28-38; Col 6, lines 10-15, 54-61; Col 13, line 40-Col 14, line 27).

15. As per claim 9, Kimmel teaches the steps of selecting a second set of computer readable instructions and repeating the acts of selecting a cluster and selecting a processor; and associating the selected processor with the second set of computer-readable instructions. (Col 11, lines 13-22; Col 9, lines 28-38; Col 6, lines 10-15, 54-61; Col 13, line 40-Col 14, line 27: clearly, the invention as disclosed by Kimmel may be repeated on all threads that need to be executed.)

16. As per claim 10, Kimmel teaches executing the first set of computer-readable instructions on the associated processor (Col 9, lines 28-38; Col 6, lines 10-15, 54-61; Col 13, line 40-Col 14, line 27).

17. As per claim 11, Kimmel teaches wherein a cluster other than the first cluster is selected if the other cluster has a processor associated with the first set of computer readable instructions and the other cluster has no processors associated with the first set of computer-readable instructions (Col 1, lines 59-67; Col 12, lines 35-55: the entire purpose of Kimmel's invention is to improve infinity, which means selecting a processor to run a thread in a thread group if it is already running other threads in the same thread group. Processors are grouped under different nodes or clusters).

18. As per claim 12, Kimmel teaches wherein a processor other than the first processor is selected if the first processor has already been associated with the first set of computer-readable instructions and the other processor has no association with the first set of computer-readable instructions (Col 1, lines 59-67; Col 12, lines 35-55).

19. As per claims 13-24, they are computer-readable medium claims of claims 1-12. Therefore, they are rejected as claims 1-12 above.

20. As per claims 25-36, they are system claims of claims 1-12. Therefore, they are rejected as claims 1-12 above.

Conclusion

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to MengYao Zhe whose telephone number is 571-272-6946. The examiner can normally be reached on Monday Through Friday, 7:30 - 5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached at 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MENG-AL T. AN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100